

The diagram illustrates a system architecture with three main components within a larger frame 204:

- Processing Unit 202 (Top Left):** Contains a microprocessor (uP) 202, RAM 208, and ROM 306.
- Processing Unit 204 (Bottom Left):** Contains a microprocessor (uP) 204, RAM 305, and ROM 207.
- Control Unit 210 (Right):** Contains a central control block 210, RAM 212, and ROM 213. It also includes a feedback loop 214.

Interconnections are shown as follows:

- Processing Unit 202 is connected to the central control block 210 via a bidirectional bus.
- Processing Unit 204 is connected to the central control block 210 via a bidirectional bus.
- The central control block 210 is connected to its own RAM 212 and ROM 213.
- A feedback loop 214 is shown connecting the output of the central control block 210 back to its input.

Fig. 3